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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/624,014	07/21/2000	Hideaki Sakaguchi	1152-0263P	4601

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EXAMINER
BARAN, MARY C

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/624,014	Applicant(s) SAKAGUCHI, HIDEAKI
	Examiner Mary Kate B Baran	Art Unit 2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-11* is/are allowed.

6)☒ Claim(s) *1-4 and 8* is/are rejected.

7)☒ Claim(s) *5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This action is responsive to amendments filed 8 January 2003. Claims 1-11 are pending. Claims 8 and 9 have been amended.

2. The amendments are sufficient to overcome the claim objections pertaining to claims 8 and 9 and the 35 U.S.C. 112, second paragraph rejections.

Specification

3. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Referring to claim 1, "A testing device for a semiconductor integrated circuit which incorporates a multiple number of D/A converters" is indefinite because it is not

clear whether the semiconductor integrated circuit or the testing device incorporates the D/A converters.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagami et al. (U.S. Patent No. 6,121,786) in view of Paulos et al. (U.S. Patent No. 6,091,350) and Ohya (U.S. Patent No. 5,745,064).

Referring to claim 1, Yamagami et al. discloses multiple voltage outputs associated with multiple voltage terminals (see Yamagami et al., column 8 lines 39-40 and Figure 5, "VREF1, VREF2, VEXT"), a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals (see Yamagami et al., column 8 lines 39-47), a multiple number of differential amplifiers (see Figure 5, "differential amplifier 7"), each having two input terminals (see Figure 5, "VREF1, VREF2, VEXT, differential amplifier 7"), one for receiving the output voltage output from the associated output terminal (see Figure 5, "VEXT") and the other for receiving the reference voltage from the reference voltage generator (see Yamagami et al., column 9 line 54 – column 10 line 2 and Figure 5, "VREF1, VREF2") and a comparator that receives the amplified output voltages from

the multiple number of differential amplifiers (see Yamagami et al., column 11 lines 24-29) and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range (see Yamagami et al., column 11 lines 39-47). Yamagami et al. does not teach multiple D/A converters which output voltages, or selectively outputting multiple sets of reference voltages.

Ohya discloses a multiple D/A converters (see Ohya, column 15 lines 12-15 and Figure 12A) which output voltages (see Ohya, column 12 lines 41-46).

Paulos et al. discloses selectively outputting a range of voltages based on a given input voltage (see Paulos et al., column 3 lines 44-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Yamagami et al. to include the teachings of Ohya because having multiple D/A converters which output voltages would have allowed the skilled artisan to reduce error (see Ohya, column 4 lines 23-27) and increase conversion speed (see Ohya, column 7 lines 59-61), and to further include the teachings of Paulos et al. because outputting a set of voltages would have allowed the skilled artisan to effectively use the available supply voltage (see Paulos et al., column 1 line 66 – column 2 line 3).

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagami et al. (U.S. Patent No. 6,121,786) in view of Paulos et al. (U.S. Patent No. 6,091,350) and Ohya (U.S. Patent No. 5,745,064), and further in view of Cheng (U.S. Patent No. 6,154,041).

Referring to claim 2, Yamagami et al. teaches outputting multiple reference voltages (see Yamagami et al., column 9 lines 50-53), but does not teach a D/A converter which receives a digital data signal different from that of the D/A converters incorporated in the semiconductor integrated circuit to generate reference voltages and can selectively output reference voltages required for testing multiple kinds of semiconductor integrated circuits, in accordance with the selection of the digital data signal.

Cheng discloses a D/A converter which receives a digital data signal different from that of the D/A converters incorporated in the semiconductor integrated circuit to generate reference voltages (see Cheng, column 5 lines 57-59) and can selectively output reference voltages (see Cheng, column 5 lines 59-60) required for testing multiple kinds of semiconductor integrated circuits, in accordance with the selection of the digital data signal (see Cheng, column 6 lines 23-36).

Paulos et al. discloses selectively outputting a range of voltages based on a given input voltage (see Paulos et al., column 3 lines 44-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Yamagami et al. to include the teachings of Cheng because using a D/A converter as a voltage generator would have allowed the skilled artisan to produce a continuous waveform (see Cheng, column 4 lines 23-27), and to further include the teachings of Paulos et al. because outputting a set of voltages would have allowed the expert artisan to effectively use the available supply voltage (see Paulos et al., column 1 line 66 – column 2 line 3).

Claims 3, 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagami et al. (U.S. Patent No. 6,121,786) in view of Ohya (U.S. Patent No. 5,745,064) and Yoshizawa et al. (U.S. Patent No. 4,980,639) (hereinafter Yoshizawa).

Referring to claim 3, Yamagami et al. discloses judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range (see Yamagami et al., column 12 line 65 – column 13 line 3). Yamagami et al. does not teach multiple D/A converters which output voltages; calculating the difference between the reference voltage generated from the reference voltage generator or the testing device and the output voltage output from each output terminal, for all the output terminals; or amplifying the values obtained from the first step.

Ohya discloses a multiple D/A converters (see Ohya, column 15 lines 12-15 and Figure 12A) which output voltages (see Ohya, column 12 lines 41-46).

Yoshizawa discloses calculating the difference between a predetermined voltage generated from the reference voltage generator or the testing device and the output voltage output from each output terminal, for all the output terminals, and amplifying the values obtained from the first step (see Yoshizawa, column 3 lines 46-59).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Yamagami et al. to include the teachings of Ohya because having multiple D/A converters which output voltages would have allowed the skilled artisan to reduce error (see Ohya, column 4 lines 23-27) and increase conversion speed (see Ohya, column 7 lines 59-61), and to further include the teachings of Yoshizawa,

because calculating and amplifying the difference would have allowed the skilled artisan to more precisely determine the output voltage of the circuit in question.

Referring to claim 4, Yamagami et al. discloses that if the output from the device varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage (see Yamagami et al., column 12 line 56 – column 13 line 3).

Referring to claim 8, Yamagami et al. discloses judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range (see Yamagami et al., column 12 line 65 – column 13 line 3) and discloses that if the output from the device varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage (see Yamagami et al., column 12 line 56 – column 13 line 3). Yamagami et al. does not teach multiple D/A converters which output voltages; calculating the difference between the reference voltage generated from the reference voltage generator or the testing device and the output voltage output from each output terminal, for all the output terminals; or amplifying the values obtained from the first step.

Ohya discloses a multiple D/A converters (see Ohya, column 15 lines 12-15 and Figure 12A) which output voltages (see Ohya, column 12 lines 41-46).

Yoshizawa discloses calculating the difference between a predetermined voltage generated from the reference voltage generator or the testing device and the output voltage output from each output terminal, for all the output terminals, and amplifying the values obtained from the first step (see Yoshizawa, column 3 lines 46-59).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Yamagami et al. to include the teachings of Ohya because having multiple D/A converters which output voltages would have allowed the skilled artisan to reduce error (see Ohya, column 4 lines 23-27) and increase conversion speed (see Ohya, column 7 lines 59-61), and to further include the teachings of Yoshizawa, because calculating and amplifying the difference would have allowed the skilled artisan to more precisely determine the output voltage of the circuit in question.

Allowable Subject Matter

7. Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 9-11 are allowed. The limitation of decreasing the width of the voltage range until the output of the amplified differential values varies is not suggested, found or taught in the prior art of record, and makes these claims allowable over the prior art.

Response to Arguments

9. Applicant's arguments filed 08 January 2003 have been fully considered but they are not persuasive. The arguments are made with reference to information taught in the specification and not with regard to limitations specified in the claims.

Applicant argues that Yamagami is not directed to a testing device for an integrated circuit. However, Yamagami teaches a self-testing integrated circuit (see Yamagami, column 4 line 66 – column 5 line 4).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sakaguchi teaches a testing device and testing method for a semiconductor integrated circuit and storage medium having the testing program stored therein.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B Baran whose telephone number is (703) 305-4474. The examiner can normally be reached on Monday - Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (703) 308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

MKB
April 2, 2003

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800